#7
04/10/03

APPENDIX
MARKED UP VERSION OF AMENDMENTS
AS REQUIRED BY RULE 121

In The Specification:

Please amend the paragraph at page 13, at lines 6-16 to read as follows:

As part of cell characterization, the characterization tool measures the responses of the cell or circuit at one or more characterization points and records those responses in the form of a characteristic equation or, alternatively, a characterization table. A characterization point refers to a specific voltage or current, temperature, and process [at] for which the tool characterizes a cell or circuit. For a given characterization point, the tool typically measures a cell's response with respect to various input transition times and capacitive loads to determine the cell's behavior. A cell's behavior refers to the way the cell or circuit's output quantity (*e.g.*, voltage) behaves as a function of its input stimulus or stimuli. For example, an AND gate behaves like a logical "and" operation. The behavior determines how a designer will use a cell or circuit, and what measurements a tool should take to predict how the cell or circuit will operate once physically implemented.

Please amend the paragraph at page 20, at lines 9-14 to read as follows:

The input file 1100 may provide the functional description of the cell or circuit in a variety of formats. For example, the input file 1100 may include a functional description of a cell in the form of the cell's Boolean specifications. The Boolean specifications may describe

combinational or sequential circuits, as desired. The Liberty (.lib) models generated according to specifications from [the] Synopsys, Incorporated (a vendor of EDA tools), constitute an example of a Boolean input file 1100.

Please amend the paragraph at page 23, at lines 4-9 to read as follows:

Note that, rather than relying on the auto-mapper 1105 to provide a characterization methodology, the user may explicitly specify the methodology, as desired. The user may do so, for example, by using the Pilot language, as described above. In other words, the user may provide via Pilot a characterization methodology that overrides the characterization methodology that auto-mapper 1105 would have selected if the user had not chosen to specify a particular characterization [characterization particular] methodology.

Please amend the paragraph at page 25, at line 16 to page 26, at line 2 to read as follows:

To characterize a CUT, in exemplary embodiments each characterization manager 1110 spawns or runs a set of *N* processes, where *N* constitutes an integer equal to or greater than unity. Each of the *N* processes corresponds to one of the simulation managers 1115A-1115N. Note, however, that one may use other arrangements for [he] the simulation managers 1115A-1115N, depending on various factors (*e.g.*, the speed, traffic level, and implementation of the coupling among the computer devices as well as the number of the computer devices), as persons of ordinary skill in the art would understand. Each of the simulation managers 1115A-1115N performs a simulation on the CUT using an input file that the characterization manager 1110

provides, as described above. Each of the simulation managers 1115A-1115N provides the results of the simulation to the characterization manager 1110.

Please amend the paragraph at page 36, at lines 15-23 to read as follows:

FIG. 10C illustrates a situation where the *D* input makes a low-to-high transition followed shortly by a high-to-low transition (shown as pulse 1248 in FIG. 10C) while the clock signal is low. Because the clock signal is low and not making a transition, the flip-flop does not transmit the transitions on the input *D* to the output *Q*. In effect, the flip-flop ignores the pulse 1248 on input *D*. The input *D* subsequently makes a [high-to-low] low-to-high transition 1250. Because that transition occurs while the clock input is high, however, the flip-flop does not transmit the transition to the output *Q*. Later, the input *D* makes a high-to-low transition 1253. Again, because the transition occurs while the clock is low, the flip-flop does not transmit it to the output *Q*. In effect, the flip-flop ignores the pulse that consists of transitions 1250 and 1253.

Please amend the paragraph at page 38, at lines 1-12 to read as follows:

As another example of the non-linear behavior of the setup and hold constraints, FIG. 13 illustrates the power consumed within a latch or flip-flop as a function of setup time. Note that, similar to intrinsic delay, power consumption increases sharply as the setup time decreases below a certain point from its nominal value. Referring again to FIG. 8B, pass gates 1218 and 1227 contend with each other as they each drive, and attempt to set, the input voltage to buffers 1221 and 1224. The contention between pass gates 1218 and 1227 results in increased power

consumption in various parts of the circuit, for example, in buffers [1218 and 1227] 1221 and 1224, as they operate in their linear regions until the resolution of the contention. At the limit, the latch or flip-flop reaches its breakdown point and power consumption within it becomes unpredictable. Note that, although FIGS. 12 and 13 show intrinsic delay and power consumption as a function of setup time, similar results apply to the hold constraint or other constraints generally.

Please amend the paragraph at page 46, at line 18 to page 47, at line 5 to read as follow:

As noted above, independent characterization of setup and hold constraints may lead to an overly optimistic meta-stable region or a negative meta-stable region. Referring to FIG. 20C, in step three, optimized constraint characterization according to the invention moves data rising edge 1330 and data falling edge 1336 away from the reference clock edge 1333 so as to widen the meta-stable region. As the edges 1330 and 1336 move away from clock edge 1333, at some point one observes a transition in the output of the latch when one simulates the behavior of the latch, *i.e.*, one obtains a valid meta-stable region. In other words, step three of the optimized constraint characterization starts with the constraint characterizations of steps one and two and moves out edges [1333] 1330 and 1336 to provide a valid meta-stable region. In exemplary embodiments of the invention, if the values of the setup and hold times acquired in steps one and two correspond to a valid meta-stable region, step three makes no adjustment to those values.

Please amend the paragraph at page 51, at lines 4-11 to read as follow:

To begin searching, inter-dependent characterization according to the invention selects values for the setup and hold constraints that correspond to the nominal delay of the cell or circuit (a point at or near the beginning of path 1365 in [FIG. 20D] FIG. 21). To select those values, one may employ any of a variety of techniques. For example, one may use a scaled value of the slowest input slew-rate applied (or expected to be applied) to the cell or circuit and use a search mechanism to find where the linear nominal delay region ends. In other words, one locates a point on the response surface 1368 where a line tangent to the surface 1368 has a slope of unity or about unity.

Please amend the paragraph at page 51, at lines 13-22 to read as follow:

One may then use a suitable search mechanism[s] to adjust the values of setup and hold in a manner that generally tends toward smaller values for setup and hold constraints. Note that generally one may use any of a variety of suitable search techniques, as desired. The search mechanism estimates through mathematical analysis, for example, by using mathematical formulae, the shape of the response surface 1368. The choice of the mathematical analysis or formulae used depends on the technology and/or design methodology used in the cell or circuit under test. The search mechanism gathers and analyzes trend data to estimate the shape (*e.g.*, the direction of change and inflection points) of the response surface 1368. In exemplary embodiments of the invention, the search mechanism uses a suitable error-estimating techniques to avoid local minima that may lead to false results.

Please amend the paragraph at page 52, at lines 1-8 to read as follow:

The search mechanism in the inter-dependent characterization technique recognizes the breakdown region of the response surface 1368 (*i.e.*, where the measurement of intrinsic delay fails) and takes measures to return the search to other parts of the response surface 1368 if it encounters the breakdown point or region. The search terminates when the search mechanism locates a valid solution point, such as point 1371 in [FIG. 20D] FIG. 21. The valid solution point 1371 provides valid values for the setup and hold constraints that represent the smallest meta-stable region found from the response surface 1368, given the search conditions that the user has established (*e.g.*, delay degradation, as described below in detail).

Please amend the paragraph at page 58, at line 19 to page 59, at line 8 to read as follow:

To generate a mirror-image plot, one pivots line 1404 around its mid-point 1407 to generate line 1410, as FIG. 25B illustrates. Put another way, line 1410 in FIG. 25B constitutes a mirror-image with respect to mid-point 1407 of line [1407] 1404 in FIG. 25A. Plot 1395 and line 1407 intersect at point 1413, as FIG. 25B illustrates. Point 1413 provides the value of the constraint determined by the normalized-intersection option according to the invention. Note that, under some circumstances, plot 1395 and line 1407 may intersect more than once. In that scenario, the user and/or the characterization tool should consistently choose one of the intersections (*e.g.*, the intersection that provides the most predictability or the intersection that results in improved performance of the cell or circuit, as desired). Note also that FIGS. 22-25 show illustrative application of the degradation options to a particular attribute, namely intrinsic

delay, although one may apply the degradation options to other attributes of a circuit or cell, for example, output slew-rate and power consumption, as desired.

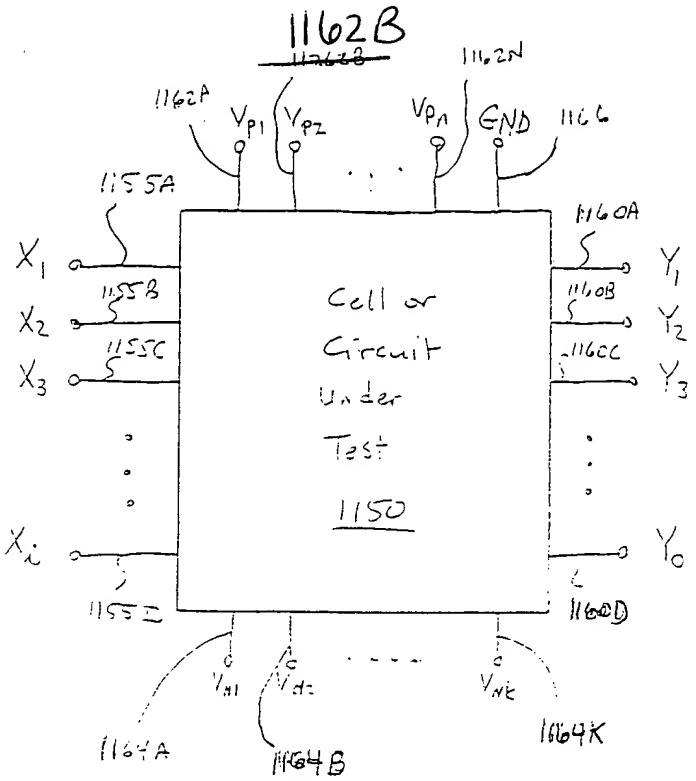

FIG. 3